Monolithic III-V active devices in-plane coupled with Si for integrated Si-photonics

The relentless growth of data traffic is rapidly approaching the communication bottleneck of Si-based integrated circuits and systems, with further scaling down hindered by technological and economic viability. Si-photonics, leveraging the highly successful Si IC infrastructure, is regarded as the enabling technology for new-generation communications as well as emerging fields, including supercomputers, neural and quantum networks, microwave photonics, and sensing. While Si-photonics has been successful with Si-based passive components, integrating III-V lasers on Si has remained the major challenge for Si-photonics. Heterogeneous integration approaches such as wafer-bonding and micro-transfer printing have facilitated the integration of high-performance III-V lasers on Si-photonics platforms. However, their integration density, cost, and manufacturing yield are suboptimal compared to monolithic integration, thereby limiting the broad adoption of Si-photonics. In the past few years, our group, along with a few others worldwide produced III-V lasers on Si by blanket epitaxy of III-V thin films on Si and incorporation of quantum dot active region. Unfortunately, the thick III-V buffer layers for defect engineering severely impede the efficient coupling between III-V active devices and Si passive components. To address this dilemma, we have developed a novel selective epitaxy method named ***lateral aspect ratio trapping (LART)***. The core concept of LART involves the ***in-plane and intimate placement of Si and III-V***, eliminating the III-V buffers and providing an elegant solution for efficient coupling between III-V and Si. The wisdom of LART also lies in the ***unique feature of removing threading dislocations (TDs)***. Traditional blanket epitaxy methods only allow for the reduction of TD density to approximately 10^6 cm^{-2} for GaAs on Si and 10^8 cm^{-2} for InP on Si using 2 to 3 μm thick III-V buffer layers. In contrast, the LART method enables the complete removal of TDs, rendering the entire III-V devices TD-free, a feat not yet achieved on any other platform.

Building upon the LART method, we have achieved TD-free III-V crystals on SOI with excellent uniformity and flexible dimensions of up to hundreds of micrometers. Furthermore, on the versatile III-V/SOI platform, we have realized high-performance photodetectors (PDs), optically pumped lasing of telecom micro-lasers arrays and distributed feedback lasers and Si-waveguide-coupled III-V PDs. In this project, we propose to advance the field by developing monolithic integration of III-V electrically pumped lasers, PDs, modulators, and Si passive devices through efficient and in-plane coupling. This program will leverage our expertise in designing novel metal-organic chemical vapor deposition (MOCVD) growth procedures, as well as laser fabrication and characterization technologies. A primary focus will be addressing the specific challenges associated with coupling high-performance III-V lasers with Si passive components on SOI – a crucial requirement for the realization of Si-photonics that has not yet been achieved on any existing platform.

The results of this project will lead to *the placement of high-performance lasers exactly where they are needed in the photonic integrated circuit in an elegant, efficient, scalable, and low-cost manner*. This unique and versatile technology will significantly contribute to the development of energy-efficient Si-photonics, yielding benefits for both academia and industry. Furthermore, it will enable the integration of cost-effective electronics and power-efficient photonics on the same chip, unlocking the next generation of datacom and telecom, fostering advancements in novel computing systems, microwave photonics, optomechanics, sensing, and LIDAR, creating new opportunities for research and innovation.